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Question Paper Code : 73442

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Third Semester

Electronics and Communication Engineering

EC 2203/EC 34/080290010/10144 EC 304 — DIGITAL ELECTRONICS

(Regulations 2008/2010)

(Common to PTEC 2203 – Digital Electronics for B.E. (Part-Time) Third Semester – ECE – Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Name the universal gates? Why are they called so.

2. Simplify $F = xy + xy'$.

3. Write the truth table for half subtractor.

4. Convert a decoder into a demultiplexer.

5. What is meant by modulus of a counter?

6. Give some basic applications of flip flops.

7. What is the disadvantage of dynamic RAM cell?

8. How PAL differs from ROM?

9. Compare mealy and moore machine.

10. List the effects due to hazards in logic circuits.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Express $F = A + B'C$ in a sum of minterms. (6)

(ii) Using Quine McCluskey method minimize the function $F = \sum(0,5,7,8,9,10,11,14,15)$. (10)

Or

(b) (i) Convert the max term expression $Y = (\overline{A} + \overline{B} + \overline{C})(A + B + \overline{C})$ to its minterm form. (6)

(ii) Simplify the logic function $F = \sum M(10,11,14,15)$ and implement using NAND gates. (10)

12. (a) (i) Explain the carry look ahead adder with a diagram. (10)

(ii) Implement the function $y = AB$ and $y = A + B$ using 2 : 1 MUX. (6)

Or

(b) Implement BCD to 7 segment code converter. (16)

13. (a) (i) Write the characteristic table, equation and excitation table of a JK flip flop and T flip flop. (6)

(ii) Design a mod 6 synchronous counter using TFFs. (10)

Or

(b) (i) What is a serial adder? Explain. (8)

(ii) With Truth table and timing diagram explain the operation of 4 bit ring counter. (8)

14. (a) (i) Describe the RAM organization and explain the write and read operations. (10)

(ii) Discuss on various types of ROM. (6)

Or

(b) (i) Implement the functions $A(x,y,z) = \sum m(1,2,4,6)$ and $B = (x, y, z) = \sum m(0,1,6,7)$ using (1) ROM (2) PLA. (8)

(ii) Outline the features of various programmable logic devices. (8)

15. (a) (i) Write the verilog HDL code for 'JK'FF and 'T'FF. (6)

(ii) An asynchronous circuit with output changing on each rising edge of its input clock. Draw the hazard free circuit. (10)

Or

(b) (i) Draw the general model of a sequential circuit and explain. (6)

(ii) List out the steps involved in the design of synchronous sequential circuit. (10)
